CLAIMS:

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. A semiconductor field-effect transistor device comprising:

a first layer of semiconductor material doped of a first dopant type;

a source region and a drain region implanted with dopants of a second opposite type;

a gate electrode separated from the first layer by a dielectric region, and positioned between said source and drain electrodes;

said substrate having one or more dislocation or crystal defects that extend continuously from the source region to the drain region, and

blocking impurity dopant materials that partially or fully occupies said dislocation defects, wherein said blocking impurity dopant materials substantially inhibit diffusion of said implanted source and drain dopants from diffusing along said dislocation or crystal defect.

2. The semiconductor field-effect transistor device as claimed in Claim 1, wherein said first layer of semiconductor material comprises material selected from the group comprising: Si, SiGe, SiGeC, or Ge.

3. The semiconductor field-effect transistor device as claimed in Claim 1, wherein said first layer of semiconductor material comprises a multi-layer structure comprising materials selected from the group comprising: Si, SiGe, SiGeC, or Ge.

4. The semiconductor field-effect transistor device as claimed in Claim 1, wherein said first layer of semiconductor material comprises a SiGe relaxed substrate.

5. The semiconductor field-effect transistor device as claimed in Claim 1, wherein said source and drain dopants of said second type comprise P, As or Sb, singly or in combination thereof, and said blocking impurity is In.

6. The semiconductor field-effect transistor device as claimed in Claim 1, wherein said source and drain dopants of said second type comprise B or In, singly or in combination thereof, and said blocking impurity is Sb.

7. The semiconductor field-effect transistor device as claimed in Claim 1, wherein said blocking impurity is a neutral-type impurity.

8. The semiconductor field-effect transistor device as claimed in Claim 7, wherein said blocking impurity is a group IV impurity.

9. The semiconductor field-effect transistor device as claimed in Claim 7, wherein said blocking impurity is C, Sn or Pb, singly or in combination thereof.

10. A method for forming a semiconductor field-effect transistor device comprising the steps of:

a) forming a first semiconductor structure comprising material doped of a first dopant type such that said semiconductor structure includes a non-zero number of threading dislocations;

b) implanting a blocking impurity in said semiconductor structure;

c) thermally processing said semiconductor structure such that said blocking impurities segregate to said existing threading dislocations, said blocking impurities further segregating to new dislocations that may be induced by said thermal processing;

d) forming a dielectric layer on top of said semiconductor structure to define a gate region, and forming a gate electrode over said dielectric region, a portion of the semiconductor structure immediately beneath the gate defining a channel region, and a portion of the semiconductor structure beneath the channel region defining a well region; and,

e) implanting dopants in said semiconductor structure on opposite sides of said gate region to form source and drain regions such that the source and drain regions abut the channel region and well region on either side,

wherein a dislocation or crystal defect extends continuously from said source to drain region, and an immediate vicinity of said crystal defect is substantially occupied by said blocking impurity dopant.

11. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said first layer of semiconductor material comprises material selected from the group comprising: Si, SiGe, SiGeC, or Ge.

12. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said step a) of forming a first semiconductor structure comprises forming a multi-layer structure comprising materials selected from the group comprising: Si, SiGe, SiGeC, or Ge.

13. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said first semiconductor structure comprises a SiGe relaxed substrate.

14. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said step b) of implanting blocking impurity dopant materials in said semiconductor structure includes implanting a blocking impurity of a concentration ranging between about $10^{17}$ $cm^{-3}$ - $10^{19}$ $cm^{-3}$.

15. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said step b) of implanting blocking impurity dopant materials in said semiconductor structure includes implanting a blocking impurity with an energy such that the peak blocking impurity concentration approximately coincides with a Si/SiGe interface.

16. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said thermally processing step c) comprises a thermal annealing step at an anneal temperature ranging between about 600 °C – 1200 °C.

17. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein dopants forming said source and drain regions comprise P, As or Sb, singly or in combination thereof, and said blocking impurity is In.

18. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein dopants forming said source and drain regions comprise B or In, singly or in combination thereof, and said blocking impurity is Sb.

19. The method for forming a semiconductor field-effect transistor device as claimed in Claim 10, wherein said blocking impurity is a neutral-type impurity.

20. The method for forming a semiconductor field-effect transistor device as claimed in Claim 18, wherein said blocking impurity is a group IV impurity.

21. The method for forming a semiconductor field-effect transistor device as claimed in Claim 18, wherein said blocking impurity is C, Sn or Pb, singly or in combination thereof.